REMARKS/ARGUMENTS

Claims 19-24 and 26 were pending in the application. All pending claims are rejected on various grounds over four applied references (*Sing et al.* (USPN 6,645,818 hereinafter "*Sing*"), *Inumiya et al.* (USPN 6,054,355 hereinafter "*Inumiya*"), *Sugawara et al.* (USPN 6,841,430 hereinafter "*Sugawara*"), and *Hammond et al.* (USPN 6,680,496 hereinafter "*Hammond*"). **Claims 19, 21, and 26 are amended herein. Claims 19-24 & 26 are now pending** and are discussed further in this application. The various grounds of rejections are discussed below.

Rejections Under 35 U.S.C. § 112

Claim 26 is rejected under 35 U.S.C. § 112, 1st paragraph, as containing subject matter not described in the specification. In response, the Applicants **amend Claim 26** to recite "forming a strained silicon channel in the gate electrode trench" and then treating the strained silicon channel with a subsequently formed "high-K film" formed thereon and later a gate electrode formed over this.

As pointed out by the Examiner, this language is supported at page 20, at lines 1-13 (hereinafter abbreviated as 20:1-13) of the specification which particularly point out and describe the relevant claim language. Optionally, "epitaxial silicon is implanted to form strained silicon in the channel" (See, 20:10-11). Also, this is "followed by deposition of the gate conductor material".

Accordingly, the applicants submit that **Claim 26** is supported by the specification and drawings and that this claim should be in allowable form as amended. Therefore, the applicants request that the present rejection of Claim 26 be withdrawn.

Rejections Under 35 U.S.C. § 103

Claims 19-24 stand rejected as unpatentable under 35 U. S. C. §§ 103(a) in view of numerous references. These references and rejections are discussed in detail below.

Claims 19 and 20

Claims 19 and 20 are rejected as unpatentable over *Sing* in view of *Inumiya*.

As to **Claim 19**, the applicants point out that *Sing* (like *Inumiya*) requires the formation of dummy gates 20 to facilitate self-aligned fabrication (See, e.g., *Sing* Figs. 5-11, and more particularly Figs 8-11). These are wasted steps that add time, effort, and cost to the process. The claimed process does not require self-aligned processes, nor does it claim them. The claimed invention foregoes such processes to obtain the thermal advantages inherent in the claimed method (See, e.g., 12:4-16 of the instant Specification). So the present invention absents the dummy gate processes required in *Sing* (see the dummy gates 20, 40, of Figs 4-10 and the discussion pertaining thereto).

This is made more clear by the amendments to Claim 19 which recite "after forming the source and drain diffusion region and after annealing and before performing other process steps, covering the planarized surface of the semiconductor substrate with a first layer of dielectric material to form a first interlayer dielectric layer on the semiconductor substrate after formation of the source and drain diffusions". This limitation addresses the added metal stack (*Sing,* 60/56/54 shown in Figs. 12, 13) required by *Sing* which the claimed invention does not require. Thus, the claimed invention claims a electrode without the need for forming the metal stack of *Sing*.

Additionally, the inventors point out that *Sing* requires the growth of the metal silicide 50 over the source drain regions (See, *Sing* e.g., at 3:60-4:4, Fig. 11) which consequently disrupts the planar nature of the top surface (as depicted in *Sing*, e.g., Fig. 11). Thus the surface upon which the dielectric layer is formed is no longer planarized as required by Claim 19.

So the present invention does not require many necessary elements of the cited art. In particular, the omission of a step to obtain the same (or in this case and improved) result is de facto indicia of non-obviousness. Accordingly, for at least this reason, the cited combination fails to teach the claimed invention.

One must look to *Inumiya* to make up the shortcomings of the *Sing*. *Inumiya* unfortunately teaches a completely different invention. Problematic of *Inumiya* is that a gate insulator film 69 is required at the bottom of the gate electrode trench. This gate insulator 69 is SiO_2 and is unlike anything required by the present invention. The claimed invention does not require such a film. As such it yet another omitted essential elements of the cited art. Accordingly, its absences is further indicia of non-obviousness.

Thus, the combination of *Sing* and *Inumiya* require steps absent from the claimed invention. Thus, the addition of the prior art dummy gates (not required by the claims) and the addition of the bottom silicon dioxide layer result in a non-functional invention which does not teach the limitations of Claim 19 (e.g., absence of self alignment features and so on) which significantly omits these steps.

Additionally, Claim 19 is amended to recite "lining the gate electrode trench and a top portion of the epitaxial layer with a high-K dielectric film". Thus, the high-K layer of the claimed invention runs over the epitaxial layer. This is not taught or suggested in the cited art.

Accordingly, for at least the reasons explained above, the applicants submit that the cited combination of references is insufficient to establish a *prima facie* case of obviousness as to Claim 19. Accordingly, applicants respectfully request that the pending ground of rejection for Claim 19 be withdrawn.

As to dependent **Claim 20**, nothing in the art cited above overcomes the deficiencies explained above in the discussion of the Claim 19 rejection. Accordingly, for at least the reasons explained above, the applicants submit that the cited combination of references is insufficient to establish a *prima facie* case of obviousness as to dependent Claim 20. Accordingly, applicants respectfully request that the pending ground of rejection for Claim 20 also be withdrawn.

Claims 21-24

Claims 21-24 are rejected as unpatentable over *Sing* in view of *Inumiya* and further in view of *Sugawara* and *Hammond*.

However, as respectfully pointed out above, the combination of *Sing* and *Inumiya* fail to teach the underlying claim limitations of base claim 19. Moreover, nothing in the cited portions of either *Sugawara* or *Hammond* address let alone overcome the deficiencies of *Sing* and *Inumiya* as explained above in the discussion of the Claim 19 rejection above. Accordingly, for at least the reasons explained above, the applicants submit that the cited combination of references is insufficient to establish a *prima facie* case of obviousness as to dependent Claims 21-24. Accordingly, for at least the reasons explained above with respect to base claim 19, the applicants submit that the cited combination of references is insufficient to establish a *prima facie* case of obviousness as to Claims 21-24.

It should also be pointed out that the high temperature processing of the "buffer layer 2" in *Sugawara* operates at almost 900°C which is hot enough for annealing problems to occur. The previous Action set forth that the applicants did not claim the 900 degree anneal temperature and ... then provides no explanation of why this comment is important or relevant. The Examiner has as much as admitted that the 900 degree temperatures required to process *Sugawara's* "buffer layer 2" are a problem. The applicants do not need to mention the precise temperatures involved. It is relevant that excessive annealing is a problem and *Sugawara's* use of it in the post anneal processing steps claimed by the present invention teach away from its combination in the rejection suggested by the Office Action. The *Sugawara* post anneal 900+ degree heating will effect the post anneal process steps claimed in Claims 21-24 and will damage the claimed structures. Thus, this combination is unsuitable for use with the claimed invention. Accordingly, for at least this added reason, the cited teaches away from the cited combination and accordingly fails to make obvious the claimed invention. Therefore, applicants respectfully request that the pending grounds of rejection for Claims 21-24 be withdrawn.

Thus, for at least these reasons, the applicants respectfully submit that the cited portions of the art fail to establish a *prima facie* case of obviousness as to Claims 19-24 and accordingly the cited art is therefore insufficient to establish an obviousness rejection under 35 U.S.C. § 103. Consequently, the applicants respectfully request that the pending grounds of rejection be withdrawn as to **Claims 19-24**.

Conclusion:

In view of the foregoing amendments and remarks, it is respectfully submitted that the claimed invention as presently presented is patentable over the art of record and that this case is now in condition for allowance.

Accordingly, the applicants request withdrawal of all pending rejections and request reconsideration of the pending application and prompt passage to issuance. As an aside, the applicants clarify that any lack of response to any of the issues raised by the Examiner is not an admission by the applicant as to the accuracy of the Examiner's assertions with respect to such issues. Accordingly, applicant's specifically reserve the right to respond to such issues at a later time during the prosecution of the present application, should such a need arise.

As always, the Examiner is cordially invited to telephone the applicants representative to discuss any matters pertaining to this case. Should the Examiner wish to contact the undersigned for any reason, the telephone numbers set out below can be used.

Additionally, if any fees are due in connection with the filing of this Amendment, the Commissioner is authorized to deduct such fees from the undersigned's Deposit Account No. 12-2252 (Order No. 03-2051).

Respectfully submitted,

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